Listing of Claims:

1. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate having a recess therein;

a gate electrode comprising a first portion in the recess and a second reduced-width portion extending from the first portion;

a source/drain region in the substrate adjacent the recess; and

a gate insulator interposed between the first portion of the gate electrode and a surface of the recess, the gate insulator comprising a first portion disposed on a sidewall of the recess, in contact with the source/drain region and having a first thickness and a second portion disposed on a bottom of the recess, spaced apart from the source/drain region and having a second thickness less than the first thickness.

2.-3. (Canceled)

4. (Previously Presented) The semiconductor device of claim 1, further comprising a nitride liner disposed between the first portion of the gate insulator and the recessed portion of the gate electrode.

5. (Previously Presented) The semiconductor device of Claim 1, further comprising:

an insulation layer on a surface of the substrate adjoining the second portion of the gate electrode above the substrate and extending over a portion of the first portion of the gate electrode; and

an insulating spacer disposed on a sidewall of the second portion of the gate electrode and on the insulation layer.

6. (Original) The semiconductor device of Claim 5, wherein the insulation layer comprises silicon oxide and the insulating spacer comprises silicon nitride.

7. (Original) The semiconductor device of Claim 5, wherein the insulating spacer comprises a first insulating spacer and further comprising a second insulating spacer on sidewalls of the insulation layer and the first insulating spacer.

8. (Original) The semiconductor device of Claim 7, wherein the source/drain region comprises a lighter-doped portion adjoining the recess.

9. (Previously Presented) The semiconductor device of Claim 1, wherein the gate electrode further comprises a third portion on the second portion, the third portion having ~~an~~ a greater width than the second portion.

10. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate having a recess therein;

a gate insulator on the substrate in the recess;

a gate electrode comprising a first portion on the gate insulator in the recess, a second reduced-width portion extending from the first portion, and a third portion on the second portion, the third portion having a greater width than the second portion;

a source/drain region in the substrate adjacent the recess;

an insulation layer on a surface of the substrate adjoining the second portion of the gate electrode above the substrate and extending over a portion of the first portion of the gate electrode; and

an insulating spacer disposed on a sidewall of the second portion of the gate electrode, on a sidewall of the third portion of the gate electrode and on the insulation layer.

11. (Original) The semiconductor device of Claim 10, wherein the insulation layer comprises silicon oxide and the insulating spacer comprises silicon nitride.

12. (Canceled)

13. (Previously Presented) The semiconductor device of Claim 9, wherein the source/drain region comprises a lighter-doped portion adjoining the first portion of the gate insulator.

14. (Canceled)

15. (Original) The semiconductor device of Claim 1, wherein the source/drain region comprises a lighter-doped portion nearer the recess.

16. (Original) The semiconductor device of Claim 1, wherein the recess has a curved shape.

17. (Original) The semiconductor device of Claim 16, wherein the recess is hemispherical or elliptical.

18.-39. (Cancelled).

40. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate having a recess therein;

a gate electrode comprising a first portion in the recess and a second reduced-width portion extending from the first portion;

a source/drain region disposed in the substrate and spaced apart from the recess; and

a substantially uniform gate insulator layer lining the recess and interposed between the first portion of the gate electrode and a portion of the substrate between the recess and the source/drain region.

41. (Previously Presented) The semiconductor device of Claim 40, further comprising:

an insulation layer on a surface of the substrate adjoining the second portion of the gate electrode above the substrate and extending over a portion of the first portion of the gate electrode; and

an insulating spacer disposed on a sidewall of the second portion of the gate electrode and on the insulation layer.

42. (Previously Presented) The semiconductor device of Claim 41, wherein the insulation layer comprises silicon oxide and the insulating spacer comprises silicon nitride.

43. (Previously Presented) The semiconductor device of Claim 41, wherein the insulating spacer comprises a first insulating spacer and further comprising a second insulating spacer on sidewalls of the insulation layer and the first insulating spacer.

44. (Previously Presented) The semiconductor device of Claim 43 wherein the source/drain region comprises a lighter-doped portion nearest the recess.

45. (Previously Presented) The semiconductor device of Claim 40, wherein the gate electrode further comprises a third portion on the second portion, the third portion having a greater width than the second portion.

46. (Previously Presented) The semiconductor device of Claim 45, further comprising:

an insulation layer on a surface of the substrate adjoining the second portion of the gate electrode above the substrate and extending over a portion of the first portion of the gate electrode; and

an insulating spacer disposed on a sidewall of the second portion of the gate electrode, on a sidewall of the third portion of the gate electrode and on the insulation layer.

47. (Previously Presented) The semiconductor device of Claim 46, wherein the insulation layer comprises silicon oxide and the insulating spacer comprises silicon nitride.

48. (Previously Presented) The semiconductor device of Claim 40, wherein the source/drain region comprises a lighter-doped portion nearer the recess.

49. (Previously Presented) The semiconductor device of Claim 40, wherein the recess has a curved shape.

50. (Previously Presented) The semiconductor device of Claim 49, wherein the recess is hemispherical or elliptical.